

Patent
52478.0700 (AN73r)AMENDMENTS TO THE CLAIMS

1 66. (New) The data processor of Claim 63, wherein the plurality of registers
2 includes at least one register storing an address exceeding 16 bits.

D1 67. (New) The data processor of Claim 64, wherein the data processor
1 performs data processing based on an 8-bit instruction, the instruction independently
2 designating:
3 one of a plurality of operations including transfer and calculation;
4 one of the registers as a source operand, and
5 one of the registers as a destination operand.

1 68. (New) A data processing method for performing data processing of an 8-
2 bit instruction, comprising
3 decoding a first portion of the 8-bit instruction which independently designates
4 one of a plurality of operations including transfer and calculation,
5 decoding a second portion of the 8-bit instruction which independently designates
6 one of a plurality of registers as a source operand,
7 decoding a third portion of the 8-bit instruction which independently designates
8 one of the plurality of registers as a destination operand.

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9 wherein at least one of the source operand register and the destination operand
10 register is capable of storing an address exceeding 16 bits; and
11 executing the instruction in accordance with the decoded results.

1 69. (New) A data processing method for performing data processing of an 8-
2 bit instruction, comprising

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3 decoding a first portion of the 8-bit instruction which independently designates
4 one of a plurality of operations including transfer and calculation.
5 decoding a second portion of the 8-bit instruction which independently designates
6 one of a plurality of registers as a source operand.
7 decoding a third portion of the 8-bit instruction which independently designates
8 one of the plurality of registers as a destination operand.

9 wherein the instruction is further followed by a linear absolute address exceeding
10 16 bits; and
11 executing the instruction in accordance with the decoded results.

1 70. (New) The data processing method of Claim 69, wherein the plurality of
2 registers includes at least one register storing an address exceeding 16 bits.

1 71. (New) A data processing method for performing data processing of an
2 instruction using a processor having a first register and a second register, comprising

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3 judging which one of sign-extending and zero-extending is to be performed on
4 operand data depending on which of the first register and the second register is
5 designated as the destination operand in the instruction, and
6 performing one of sign-extending and zero-extending on operand data which is
7 judged to be performed.

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1 72. (New) The data processing method of Claim 71, wherein the instruction is
2 an 8-bit instruction which independently designates:
3 one of a plurality of operations including transfer and calculation;
4 one of a plurality of registers as a source operand, and
5 one of the plurality of registers as a destination operand;
6 the data processing method further comprising:
7 decoding a first portion of the 8-bit instruction which independently designates
8 one of a plurality of operations including transfer and calculation,
9 decoding a second portion of the 8-bit instruction which independently designates
10 one of a plurality of registers as a source operand, and
11 decoding a third portion of the 8-bit instruction which independently designates
12 one of the plurality of registers as a destination operand, and
13 executing the instruction in accordance with the decoded results, including
14 performing one of sign-extending and zero-extending which is judged to be performed.

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1 73. (New) A data processing method for performing data processing of an 8-
2 bit instruction, comprising

3 decoding a first portion of the 8-bit instruction which independently designates
4 one of a plurality of operations including transfer and calculation.

5 decoding a second portion of the 8-bit instruction which independently designates
6 one of a plurality of registers as a source operand.

7 decoding a third portion of the 8-bit instruction which independently designates
8 one of the plurality of registers as a destination operand.

9 wherin an address register and a data register are included in the plurality of
10 registers, and an address stored in the address register is longer than data stored in the
11 data register; and

12 executing the instruction in accordance with the decoded results.

1 74. (New) A recording medium recording machine readable program
2 instructions executed by a processor, the processor performing data processing of an 8-bit
3 instruction comprising

4 a first portion which independently designates one of a plurality of operations
5 including transfer and calculation.

6 a second portion which independently designates one of a plurality of registers as
7 a source operand, and

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8 a third portion of the 8-bit instruction which independently designates one of the
9 plurality of registers as a destination operand.

10 wherein at least one of the source operand register and the destination operand
11 register is capable of storing an address exceeding 16 bits.

1 75. (New) A recording medium recording machine readable program
2 instructions executed by a processor, the processor performing data processing of an 8-bit
3 instruction comprising

4 a first portion which independently designates one of a plurality of operations
5 including transfer and calculation,

6 a second portion which independently designates one of a plurality of registers as
7 a source operand, and

8 a third portion of the 8-bit instruction which independently designates one of the
9 plurality of registers as a destination operand.

10 wherein the instruction is further followed by a linear absolute address exceeding
11 16 bits.

1 76. (New) The recording medium of Claim 75, wherein the plurality of
2 registers includes at least one register storing an address exceeding 16 bits.

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1 77. (New) A recording medium recording machine readable program
2 instructions executed by a processor, the processor performing data processing of an 8-bit
3 instruction, the 8-bit instruction comprising:

4 a designation of one of a first register and a second register as containing a
5 destination operand for the instruction,

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6 wherein a judgment of which one of sign-extending and zero-extending is to be
7 performed on operand data is made depending on which of the first register and the
8 second register is designated as the destination operand in the instruction.

1 78. (New) The recording medium of Claim 77, wherein the 8-bit instruction
2 further comprises:

3 a first portion which independently designates one of a plurality of operations
4 including transfer and calculation,

5 a second portion which independently designates one of a plurality of registers as
6 a source operand, and

7 a third portion of the 8-bit instruction which independently designates one of the
8 plurality of registers as a destination operand,

9 wherein the first register and the second register are included in the plurality of
10 registers.

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1 79. (New) A recording medium recording machine readable program
2 instructions executed by a processor, the processor having a plurality of registers, the
3 processor performing data processing of an 8-bit instruction comprising:

4 a first portion which independently designates one of a plurality of operations
5 including transfer and calculation,

6 a second portion which independently designates one of a plurality of registers as
7 a source operand, and

8 a third portion of the 8-bit instruction which independently designates one of the
9 plurality of registers as a destination operand,

10 wherein an address register and a data register are included in the plurality of
11 registers, and an address stored in the address register is longer than data stored in the
12 data register.
